REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

I. Disposition of Claims

Claims 1-36 are pending in this application. Claims 1, 10, 19, and 28 are independent. The remaining claims depend, directly or indirectly, from claims 1, 10, 19, and 28.

II. Rejection under 35 U.S.C § 102

Claims 1-9 and 19-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,446,188 ("Henderson"). This rejection is respectfully traversed.

The present invention relates to a computer system, including a processor, an object cache, a memory, and a translator. In particular, the translator is interposed between the object cache and the memory. Further, the translator maps an object address to a physical address within the memory. Additionally, the present invention is implemented entirely in hardware.

On the other hand, Henderson discloses a system for mapping sparsely populated virtual space of memory objects to more densely populated physical address space. The system as taught by Henderson uses an object cache and an object manager having an address translation table. (See col. 3, ll. 5-28.)

As shown in Figure 3A, the address translation table as taught by Henderson translates virtual space addresses for memory objects to physical space addresses. In other embodiments, the address translation table (324 in Figure 3B), in addition to management table, uses caching associative memories. (See col. 6, ll. 11-14.) Further, in another embodiment, the address

translation table is referred to as an address translation module (402 in Figure 4 and col. 6, ll. 60 and 61).

Despite the various embodiments of the address translation table as shown in Figures 3A, 3B, and 4, the address translation table is *not* "interposed between the object cache and the memory," as required by claim 1. In fact, in the various embodiments, the address translation table (or module) is shown to be located between the processor and the object cache. (Please *see* Figures 3A, 3B, and 4.) Therefore, Henderson *fails to* disclose the claimed invention.

Further, the method for retrieving an object from memory as recited in claims 19 and 28 of the present invention is not disclosed by Henderson. In particular, the location of the address translation table as taught by Henderson requires that all virtual addresses are translated into a physical space addresses. Henderson states:

> The present invention comprises a host processor virtual address space 304 for storing the memory objects 308A, 308B, and 308C, that are used by the CPU or host processor. Each memory object is mapped to one or more memory elements located in the physical system memory 306...The virtual space address of the memory object 308 used by the host processor is inputted to the DMC 102 for translation by the address translation module 310 (col. 5, ll. 18-27).

In other words, each virtual address of an object is translated by the address translation table into a physical address.

In contrast, claims 19 and 28 recite "translating the object address into a physical address *if* the object address is not in the tag array" (emphasis added). The location of the translator in the present invention is interposed between the object cache and the memory. Therefore, if, and only if, the object address is not present in a cache, then the object address is translated into a physical address. (See instant specification p. 7.) Advantageously, the invention allows objects

to be relocated within the memory without modifying all references to the objects. (See instant specification, p. 10.)

However, Henderson does not disclose the translating as a conditional step, such as "if the object address is not in the tag array," as recited in claims 19 and 28. Further, Henderson does not suggest that the translation is conditional because the address translation table is located between the processor and the object cache, which does not allow a determination of whether or not a virtual address is in the object cache before a virtual address is translated. Therefore, Henderson *fails to* disclose all of the elements of claims 19 and 28.

Because Henderson does not disclose or suggest all of the limitations of claims 1, 19, and 28, Henderson cannot anticipate the invention as recited in claims 1, 19, and 28. Claims 2-9, 20-27, and 29-36, being dependent, are likewise patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

III. Rejection under 35 U.S.C § 103

Claims 10-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0178341 ("Frank") in view Henderson. This rejection is respectfully traversed.

Frank discloses a system and method for indexing and retrieving objects stored in a cache. As indicated by the Examiner, Frank does not disclose, "a translator interposed between the object cache and the memory," as required by claim 10. Further, as described above, Henderson fails to provide that which Frank lacks, namely a translator, which is interposed between the object cache and the memory. Therefore, claim 10 is patentable over Frank and Henderson, whether considered separately or in combination. Dependent claims 11-18 are

likewise patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply to be fully responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 16159/072001).

Respectfully submitted,

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